03-23-00

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Docket No.: 041-481-RB

Date: March 21, 2000

Assistant Commissioner for Patents
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of Inventor(s):

JORGE HUMBERTO FIGUEREDO

Note: A patent must be applied for in the name(s) of all of the actual inventor(s). 37 CFR 1.41

For:

METHOD FOR TESTING MULTI-CHIP PACKAGES

Enclosed are:

1. **The Papers Required for Filing Date Under 37 CFR 1.53(b)**:

26	Pages of specification
1	Pages of Abstract
6	Pages of claims
7	Sheets of drawings
	formal
X	informal

In addition to the above papers, there is also attached:

_____ Pages of an amendment _____

CERTIFICATION UNDER 37 CFR 1.10

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on this date, March 21, 2000, in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number EL070486814US addressed to: Box Patent Application, Assistant Commissioner for Patents , Washington, D.C. 20231.

Patti S. Preddy
(Type or print name of person mailing paper)

Patti S. Preddy
(Signature of person mailing paper

NOTE: Each paper or fee referred to as enclosed herein has the number of the "Express Mail" mailing label placed thereon prior to mailing. 37 CFR 1.10(b).

2. Declaration or oath

__X__ Enclosed

__X__ original

executed by (check all applicable boxes)

__X__ inventors(s)

_____ legal representative of inventor(s) 37 CFR 1.42 or 1.43

_____ joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached.

_____ This is the petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 also attached. See item 7 below for fee.

_____ Not enclosed

NOTE: Where the filing is a completion in the U.S. of an international application under 35 U.S.C. 371(c)(4), the declaration must be filed.

_____ Application is made by a person authorized under 37 CFR 1.41(c) on behalf of all of the above-named inventors(s). The declaration or oath, along with the surcharge required by 37 CFR 1.16(e) can be filed subsequently.

NOTE: It is important that all the correct inventors(s) are named for filing under CFR 1.41(c) and 1.53(b).

_____ Showing that the filing is authorized. (Not required unless called into question. 37 CFR 1.141(d).

3. Language

__X__ English

_____ non-English

NOTE: An application including a signed oath or declaration may be filed in a language other than English. A verified English translation of the non-English language application and the processing fee of $20.00 required by 37 CFR 1.17(K) is required to be filed with the application or within such time as may be set by the Office. 37 CFR 1.52(d).

NOTE: A non-English oath or declaration in the form provided or approved by the PTO need not be translated. 37CFR1.60(b).

_____ A verified English translation of the specification is attached.

4. Assignment

__X__ An assignment of the invention to __UNISYS CORPORATION__

5. Certified Copy

_____ A certified copy of application(s) from which priority is claimed.

NOTE: Must be referred to in oath or declaration. 37CFR1.55 and 1.63.

6. **Fee Calculation**

CLAIMS AS FILED

Number Filed	Number Extra	Rate	Basic Fee $690.00
Total Claims -10- -20=	-0- X	$ 18.00	-0-
Independent Claims -5- -3=	-2- X	$ 78.00	156.00
Multiple dependent claim(s) if any -0-	-0- X	$260.00	-0-

_____ Amendment canceling extra claims enclosed

_____ Amendment deleting multiple dependencies enclosed

_____ Fee for extra claims not being paid at this time

NOTE: If the fees for extra claims are not paid on filing, they must be paid or the claims canceled by amendment prior to the expiration of time period set for response by the Patent and Trademark Office in any notice of fee deficiency.
37 CFR 1.16(d)

Filing Fee Calculation $ 846.00

7. **Small Entity Statement**

_____ verified statement that this is a filing by a small entity under 37 CFR 1.9 and 1.27 is attached.

Filing Fee Calculation (50% of above) $_____

8. **Fee Payment Being Made At This Time**

_____ Not Enclosed

_____ No filing fee is to be paid at this time. This and the surcharge required by 37 CFR 1.6(e) can be paid subsequently.

NOTE: Where the filing is completion in the U.S. of an international application, the fee must be paid.

__X__ Enclosed

__X__ basic filing fee $846.00

__X__ recording assignment $ 40.00
(40.00 37CFR 1.21(h)(j)

_____ petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached. ($130.00 37 CFR 1.47 and 1.17(h) $_____

_____	for processing an application with a specification in a non-English language ($20.00; 37 CFR 1.53(d) and 1.17(k)	$_____
_____	processing and retention fee $100.00; 37 CFR 1.21(l)	$_____

NOTE: 37 CFR 1.21(l) establishes a fee for processing and retaining any application which is abandoned for failing to complete the application pursuant to 37 CFR 1.53(d) and this, as well as the changes to 37 CFR 1.53 and 1.78 indicate that in order to obtain the benefit of a prior U.S. application, either the basic filing fee or the processing and retention fee of §1.21(l) within one year from notification under § 53(d) must be paid.

Total fees enclosed $886.00

9. Method of Payment of Fees

_____ check in the amount of $_____

__X__ charge Account No. 19-3790 in the amount of $886.00. A duplicate of this transmittal is attached.

NOTE: Fees should be itemized in such a manner that it is clear for which purpose the fees are paid. 37 CFR 1.22(b)

10. Authorization to Charge Additional Fees

NOTE: If no fees are to be paid on filing, the following items should **not** be completed.

WARNING: If these boxes are to be checked, then accurately count claims, especially multiple dependent claims, to avoid unexpected high charges.

__X__ The Commissioner is hereby authorized to charge the following additional fees which may be require to Account No. 19-3790 .

__X__ 37 CFR 1.16 (filing fees and presentation of extra claims)

_____ 37 CFR 1.17 (application processing fees)

_____ 37 CFR 1.18 (issue fee at or before Mailing of Notice of Allowance, pursuant to 37 CFR 1.31(b).

NOTE: 37 CFR 1.28(b) requires "Notification of any change in loss of entitlement to small entity status must be filed in the application ...prior to pay...issue fee."

11. Instructions As To Overpayment

__X__ credit Account No. 19-3790

_____ refund

Alfred W. Kozak
Signature of Attorney

Reg. No. 24,265

Tel No. (858) 451-4615

Alfred W. Kozak
(Type or print name of attorney)

Unisys Corporation
10850 Via Frontera, MS 1000
San Diego, CA 92127

TITLE: METHOD FOR TESTING MULTI-CHIP PACKAGES

FIELD OF THE INVENTION:

This disclosure concerns specialized methods for testing multi-chip packages in order to detect short-circuits on internal components without the need to open the part involved. This method can also be used to test parts on circuit boards.

BACKGROUND OF THE INVENTION:

With the continued expansion of digital technology, more and more attention is being placed and developed on the digital circuitry components which are often found in multi-chip packages. Because of the miniature nature of the components within the multi-chip packages, it is essential that operational testing be effectuated in order to ensure the workability and reliability of a given package. These packages are actually manufactured using multi-layer printed circuit board elements that have materials which could be combustible.

Even after the normal testing methods have been used on the multi-chip packages, it was often found that some of the package parts would actually burst into flames right on the boards of the customers' product. The fact that there were certain bad parts in the packages which could fail with later use was not easy to detect because, for example, in order to detect a possible short-circuit within the package it was normally necessary to power-up the package and run the risk of burning the entire part.

The short circuits that cause parts to burst into flames were often found on the power bus and because of the already-low resistance of the power bus, it was very difficult, if not impractical, to detect any potential shorts.

It was often more difficult to detect or test the parts which were already placed on the boards. For example, there may be four packages on each board (multi-chip packages), plus also the extra components already on the printed circuit board. It was most desirable to conceive and find some method or system for testing these multi-chip packages before they were delivered for use to

a customer in order to ensure reliability and safety factors which might be involved.

As a result, it was conceived that there was the possibility of monitoring the resistance (across the power bus) versus the temperature on a multi-chip package, which could possibly provide a way to detect potential internal shorts even while the packages were mounted on the printed circuit boards. It had been found that the short-circuitry on the internal parts were a result of poor contacts caused by excessive conductive epoxy which would later become short circuits when exposed to heat. It was then seen that monitoring the power bus resistance versus the temperature of a multi-chip package, here could be a way to detect potential short-circuits even when the packages were mounted on printed circuit boards.

It was understood that the normal bus resistance offered a rather linear change against temperature. It was expected that poor or shorted contacts would have an erratic behavior when exposed to heat and therefore, it was possible that by monitoring the total resistance of the power bus that any non-linear component should then be detectable.

As a result of a devised method, it was then found possible to detect short-circuits on components that were normally conceived to have an undetectable effect on the power bus. Thus, just about any component connected directly or indirectly between the internal power bus and ground would have an influence on the power bus resistance to ground and especially so if the component was shorted directly or intermittently by the epoxy used to mount the component. Thus the power bus to ground resistance could indicate a problem at any given temperature of the package.

As a result of the above concepts, the multi-chip circuit package components on the printed circuit

boards could be tested without the need to remove them from the printed circuit board, thus saving much time and expense.

SUMMARY OF THE INVENTION:

A Device Under Test (DUT) such as a multi-chip module is placed adjunct to an aluminum temperature Transfer Block. The aluminum Transfer Block is placed against a Peltier Thermal Electric Module, which is used as a heat pump and utilizes what is called the "Peltier" effect to move heat, as if it were a thermal electric cooler. The Peltier Thermal Electric Module is attached to a heat sink and fan.

A digital multi-meter is connected to a test socket for sensing the resistance occurring between a power bus (VCC) and ground, while a temperature meter is connected to the aluminum temperature Transfer Block. A programmable power supply controlled by a computer program is connected to regulate the Peltier Thermal Electric Module and a computer-controlled fan power supply regulates the fan above the heat sink above the Thermal Electric Module.

A personal computer is used to control the above modules in order to cycle an increasing temperature ramp followed by a decreasing ramp. A meter is used to read the Vcc to ground resistance as a function of the temperature change that occurs.

As a result of cycling the voltage-to-ground resistance and reading-out the relative temperature ramp changes, there is found to be a distinctive graph pattern between a module which is normal in operation and a module which has internal intermittent or complete electrical shorts or has a high potential of becoming inoperative.

BRIEF DESCRIPTION OF THE DRAWINGS:

Fig. 1 is a diagram of the test set-up showing the modules involved for connecting to and monitoring the Device Under Test;

Fig. 2A is a view of a component from a multiple-chip Device Under Test which indicates how excess conductive epoxy can cause components to fail or result in a short-circuit;

Fig. 2B is a schematic drawing showing how a component such as a miniscule capacitor is mounted via conductive epoxy and connected for a test run;

Fig. 3A is a drawing showing the test results of a defective part with an intermittent short showing the type of pattern when the voltage-to-ground resistance is measured against the relative temperature change during a ramp-up and ramp-down cycle; Fig. 3B shows the graph of the same part after removal of the short;

Fig. 4 is another drawing showing a test-run indicating the resistance change as the temperature of the tested module is increased and decreased, so that the relative temperature change provides a specialized resistance pattern which indicates a defective epoxy contact;

Fig. 5 is a diagram showing a normal or proper result, as for example, after the repair of the defective epoxy contact, such that a very distinct characteristic almost linear resistance pattern is shown when the change in voltage-to-ground resistance is plotted against the relative temperature change which is cycled up and then down;

Fig. 6, (involving Figs. 6A and 6B), is a flow chart illustrating the steps involved in exercising the device under test in a series of up ramp temperatures and down ramp temperatures, while continually measuring the power bus to ground resistance.

DESCRIPTION OF PREFERRED EMBODIMENT:

Referring to Fig. 1, a multi-chip package which is designated as a Device Under Test 28, is seen connected to a test socket 30. The test socket 30 is connected to a digital multi-meter in order to monitor the resistance between two connections of the Device Under Test.

Placed upon the Device Under Test is an aluminum temperature Transfer Block 26, which is connected to a temperature meter 14 which can read the temperature of the aluminum temperature Transfer Block. Above, connected directly to the aluminum temperature Transfer Block, is a Peltier Thermal Electric Module 24 which is connected and regulated by a programmable power supply 16 controlled by the computer. Then, a heat sink 22 connects adjacent to the Peltier Thermal Electric Module and is supplied with a fan unit 20 which is controlled by a computer-controlled fan power supply 18.

Each of the modules 12, 14, 16, and 18, are controlled by software designed for this test. The software runs in a personal computer 10 shown providing control lines to each of these units.

A significant use in the test method is the use of a Thermal Electric Module 24 which uses the Peltier effect. The Peltier module involves the use of a flowing current, so that when a current flows across the junction of two unlike metals, this gives rise to either an absorption of heat or a liberation of heat. If the current flows in the same direction as the current at the hot junction of a thermal electric circuit of two metals, then heat is absorbed; if the current flows in the same direction as the current at the cold junction of the thermal electric circuit, then heat is liberated. The heat developed in a junction of two metals is proportional to the first power of the current, and of

course, depends on the direction of the current. This feature enables control to be applied in order to develop heat to cause an increasing temperature ramp or to absorb heat to cause a cooling temperature ramp.

A Thermal Electric Module is a small solid-state device that can operate as a heat pump or as an electrical power generator. When used to generate electricity, the module is called a "Thermal Electric Generator" (TEG) when used as a heat pump, the module utilizes the Peltier effect to move heat and is called a "Thermal Electric Cooler" (TEC).

The Thermal Electric Cooler consists of a number of p and n-type pairs or couples connected electrically in series and sandwiched between two plates. When connected to a DC power source, current causes the heat to move from one side of the thermal electric couple to the other. This creates a hot side on one side, and a cold side on the other side of the Thermal Electric Module. In a typical application, the cold side of the thermal electric module is exposed to the object or substance to be cooled, while the hot side is exposed to a heat sink which dissipates the heat to the environment.

The Thermal Electric Cooler (TEC) is a DC device. The amount of heat pumped through the TEC is directly proportional to the power supplied, and the temperature can be controlled through manual or automatic means. An automatic controller can range from a simple on-off thermostat to a complex computer-controlled feedback circuit which is done in the present testing method.

Thus, as was indicated in Fig. 1, a varying resistance of the component (which is connected between a power bus and ground) is measured via the test socket 30 from digital multi-meter 12. The Device Under Test 28 will then be subject to various levels of heat, as

measured by the temperature meter 14 at the aluminum temperature Transfer Block 26. Here, the Peltier Thermal Electric Module 24, which is under control of the programmable power supply 16, add in or remove the heat via the heat sink 22. During this operation, the temperature meter 14 will be able to monitor and check the temperature condition of the Device Under Test 28 as the test socket 30 monitors the resistance across the component in the package.

Then, as a result of the test pattern generated by sequencing the temperature a lower range to a higher range and vice versa and reading-out the resultant resistance variations, it can then be easily and readily verified as to whether the Device Under Test is properly operating without short-circuits or whether there are erratic or intermittent shorts occurring within the package.

Fig. 2A is an expanded sized illustration of a surface mount component which is inserted in a multi-chip integrated circuit, and one particular component is illustrated here as an example. For example, this surface mount component may be a capacitor which is of miniscule size such as one-eighth of an inch square. This tiny component will have metallic electrically conducting strips at each end and each end is then attached with conductive epoxy in order to make a proper electrical contact to terminals on the integrated circuit board. The upper illustration of Fig. 2A shows a properly mounted component in which the correct amount of epoxy to hold and electrically connect the service mount component to the connective terminals on the circuit board is illustrated.

Then the lower drawing in Fig. 2A shows an excessive amount of conductive epoxy having been applied to the end terminal metallic surfaces with the result of a spreading of the epoxy in an excessive manner thus

causing in a short circuit of the internal component which in this case is illustrated as a capacitor. When this occurs, this particular surface mount component will be unable to serve its purpose and the epoxy short will overheat and may even burst into flame.

Now referring to Fig. 2B, an illustrative schematic is shown to illustrate some typical conditions of the multi-chip package 28.

The multi-chip package 28 is considered the device under test DUT. Running through the package is a power bus 40 which provides the collector voltage to various elements on the package. There may be a series of multiple chips connected to the power bus such as an integrated circuit 44, an integrated circuit 46, and an integrated circuit 48.

Then there are other components attached or connected to the power bus voltage and these are illustrated as specialized mounted components 29a, 39a, and 49a. In the illustration of Fig. 2B, these components are shown as capacitative elements wherein a capacitance is provided from the power bus 40 to the ground connection 42. Then for illustrative purposes, the component 29a is shown to have conductive epoxy 29x connected to the terminal pads 29b and 29c. The conductive epoxy 29x provides the electrical connection and mechanical holding connection of the component to the terminal pads 29b and 29c. However, should there be a spread of epoxy between the terminal pad 29b and 29c then, of course, there is a short circuit involved which will obviate the effect of the internal capacitance and nullify the action of the multi-chip package.

It should be emphasized that these components, such as 29a, 39 and 49 are very tiny components often less than one-eighth of an inch square in size, and a very delicate operation is required in order to apply the proper amount of epoxy to make the electrical contact to

the interconnecting pads without causing an excessive spread of epoxy which may short the component.

However, when such a multi-chip package is sealed there is no way ordinarily to tell what operating conditions are involved during power up and electrical operations.

However, the present testing method will utilize a procedure which will monitor the incremental resistance from the power bus to ground caused by the relative temperature change of the DUT. The power bus to ground resistance increases with each temperature increment.

TEST SEQUENCE: The device under test, that is to say the multi-chip package 28, is connected to a test socket 30 (Fig. 1) and an aluminum temperature Transfer Block 26.

The device under test is subjected to a temperature rise of about 20 to 30 degrees Celsius from room temperature and then returned back to room temperature while there is a monitoring of the Vcc to ground resistance of the device under test. The purpose and effect of the test is to detect non-linearity regarding the Vcc to ground resistance versus the temperature. Now referring to Fig. 1, a particular part number of the device is entered into the personal computer 10 while the device under test 28 is placed onto the test socket 30. The operator then presses a key on the computer in order to start the test. For example, by using a range of 20 degrees for the ramp temperature span, the up-ramp and down-ramp temperature cycle can be accomplished in less than 15 minutes for a complete test cycle.

The computer verifies that the DUT is properly inserted by monitoring the Vcc to ground resistance on that particular part. There is software in the computer to conduct the test and plot results.

Now, if the continuity test passes to show that the device under test has been properly connected, then the personal computer 10 initiates the test by ramping up the temperature of the device under test 28 by utilizing the thermal electric module assembly 24 and the programmable power supply 16. In this situation, the programmable power supply will pass current through the Peltier thermal electrical module 24 in order to generate heat. This heat is then passed through the aluminum temperature Transfer Block 26 over to the device under test.

Of course, while this is happening, the test that circuit 30 connected to multimeter 12 then reads out the ohms of resistance between the power bus and ground related to the particular component of the multi-chip module which is under test.

A computer program (test program) controls the amount of power delivered to the thermal electric module (Peltier module) in order to approximate a straight line for the temperature rise.

Then the computer controls the cooling of the thermal electric module 24 by reversing the power to the thermoelectric module and controlling a cooling fan 20 to cause the temperature to drop on an approximate straight line.

As was previously mentioned, the Peltier thermal electric module controls a junction of two dissimilar metals wherein current in one direction will cause a heating effect while current in the opposite direction will cause a cooling effect.

Subsequently, when the temperature reaches down to room temperature, that is to say the starting temperature that was involved, then the test is terminated.

During the test, the Vcc to ground resistance is constantly monitored along with a temperature change.

These parameters are then plotted on the computer monitor screen for evaluation and also at the same time is saved in a file for future reference.

The programmable power supply 16, the temperature meter 14, a thermal electric Peltier module 24, and a computer 10 are components of a servo loop. This servo loop allows the computer to control the up and the down ramping of the test temperature, in essence to try to follow a rather linear rise and a linear fall. The temperature meter 14 is used as feedback for the servo loop. The digital multimeter 12 is used to measure and collect the Vcc to ground resistance of device under test (DUT) during the test program.

The fan power supply 18 allows the computer 10 to control the on-off state of the fan 20. The fan is turned off when the tester is idle and turned on during the testing operation.

The personal computer 10 is used to control the testing operations by first ramping the temperature up and then ramping the temperature down on the device under test all the while monitoring the resistance involved from the power bus Vcc to ground. Here the computer 10 collects, saves, and plots the data for evaluation. Additionally, the computer 10 will be used to prompt the operator on the required actions.

The fan 20 is used to help thermal electric module 24 maintain room temperature on the external side for faster response. The heat sink 22 is used to help the fan do a faster temperature transfer, that is to say, provide air to the thermal electric module and then vent the thermal electric module to air.

The Peltier thermal electric module 24 is used as a heat pump because it is easy to control and use, and it is easy to control also by a computer such as the computer 10. Further, it is easy to connect and easy to reverse its action from a heating to a cooling operation

by just switching the power supply polarity from the programmable power supply 16.

The aluminum temperature Transfer Block 26 is used as an interface between the device under test 28 and the Peltier thermal electric module 24. The thermal electric module is generally made of two thin square pieces of ceramic. The test socket 30 is of the zero insertion force type and due to the high pin count of the device under test, it is necessary to use this type of socket in order to prevent damage to the device under test 28.

Fig. 3A is an example of an output graph which would indicate a defective part (designated W1008) having an intermittent short. Here it is noted that at the start of the test with the relative temperature being approximately ramped up from over a range of 20 to 30 degrees Celsius, it is seen that the power bus to ground resistance will rise then suddenly deteriorate and then return up to a higher level and eventually drop down to a lower level. Fig. 3B shows the same test cycle (of part W1008) after removal of the short to show a smooth straight line graph.

Referring to Fig. 4, there is shown a ramp up of temperature range from 20 to 30 degrees Celsius and a ramp down of temperature range from 20 to 30 degrees Celsius wherein the power bus to ground resistance in ohms has a lesser slope on the ramp up and a higher slope on the ramp down which indicates another type of defect such as bad epoxy contact within a component of the multi-chip package.

Now, Fig. 5 is an illustration of a 20 to 30 degree range Celsius ramp up and ramp down in temperature which indicates that the power bus to ground resistance follows a steady slope on the up ramp and a similar slope on the down ramp of temperature, so that there is an indication that the internal component is working in

proper condition without any shorts or bad electrical contacts.

In Figures 3, 4, and 5, the 7.8 to 7.9 ohm resistance values are the result of the large number of higher value resistive components connected in parallel across the power bus to ground.

The normal room temperature was selected as the starting point for a number of reasons. These include:

(a) To have a consistent and repetitive test with a standard starting point;

(b) To prevent other temperature effects from affecting the tests, such as thermal expansion of mechanical parts;

(c) The Peltier thermal electric module has a maximum operating temperature of 150 degrees Celsius.

(d) The epoxy which is used to attach the components to the integrated circuit package is also limited to a relatively low maximum temperature, so that starting from room temperature to a ramp up and increase of 20 to 30 degrees would not be too severe in straining the integrated circuit package.

Fig. 6 (which includes 6A and 6B) is a flow chart which illustrates the programmatic steps undertaken by the computer 10 internal program which controls and senses the various elements of the apparatus shown in Fig. 1.

Step A of Fig. 6A is the initial step for checking the temperature of the Transfer Block 26 of Fig. 1.

At step B, the Transfer Block 26 is checked to insure that it is at room temperature and therefore ready

for use in testing another component-package. The Transfer Block temperature will be brought to room temperature, if necessary, by the programmable power supply 16 which operates on the Peltier thermal electric module 24.

If the Transfer Block temperature 26 is determined to be higher or over the room temperature, then step B2 is invoked in order to decrease the Transfer Block temperature 26 down to room temperature, and this is also accomplished by the programmable power supply 16 which operates on the Peltier thermal electric module 24 in order to cause a cooling or endothermic effect to take place.

If the Transfer Block is found to be at room temperature by the temperature meter 14 of Fig. 1, then the device under test 28 is inserted into the test socket 30 of Fig. 1. When this occurs, the digital multimeter 12 will now be able to check the power bus voltage to ground resistance (Vcc to ground).

This is accomplished at step E, whereby the digital multimeter 12 will be able to measure the power bus to ground resistance during the temperature ramps.

At step F, a check is made for an open circuit which if it is indicated as "Yes", then at step F1 a prompt is given to indicate that the device under test (DUT) cannot be detected. Thus, the device may not be properly inserted or else open-circuited.

At step F, if there is not an open circuit which indicates some resistance, then the indication is "No" in order to proceed to step G.

At step G, a test is made to indicate whether the power bus to ground is shorted. If this indicates "Yes" the program then proceeds to step G1 where an indication is given that the device under test is shorted and should be removed.

At step G, if no short has been indicated, then the testing process may now proceed on a normal basis. At step H, the monitoring will occur of the DUT 28 (device under test resistance), and also the condition of its temperature every two seconds.

Step H (Fig. 6B) initiates a sequential loop utilizing steps H, I, J where a logging cycle (of temperature and resistance) occurs every 2 seconds during Step I which increases the temperature in 2 degree steps until at step J the temperature has reached a 20 degree change from room temperature. For each NO at step J, the loop continues until the 20 degree change indicates a YES, which then sequences to step K.

At step I, the temperature of the device under test is increased upward over a range of 20° on the basis of 2° per minute. This is done by the programmable power supply 16 which is applied to the Peltier thermal electric module and the aluminum temperature Transfer Block 26 which is attached to the device under test (DUT) 28.

Then at step J, when the temperature has reached a span of +20° from the starting point (Yes), then the computer 10 will monitor the device under test (DUT) 28 resistance and temperature and log out a reading every two seconds during the temperature down ramp which is sequenced through steps K, L and M.

Then steps K, L and M operate as a sequencing loop to log the temperature and resistance while reducing the temperature of the DUT back to room temperature at the rate of 2 degrees per minute.. The loop sequence K-L-M repeats until the Transfer Block 26 and the DUT 28 return to room temperature (YES).

Thus, at step L, the temperature is decreased downward over a range of 20° also at the rate of 2° per minute. This is controlled by the temperature meter 14, the programmable power supply 16, the fan power supply

18, and a digital multimeter 12,all under the control of the program in the personal computer 10.

Then at step M, "YES" the down ramp temperature cycle has been completed and the temperature had been reduced by 20° from its peak.

Then Fig. 5A shows step N indicating termination of the test and need to remove the DUT 28. A signal is then sent to step A to check the Transfer Block temperature in order to verify it is then at the room temperature, and ready for another DUT to be tested.

During this period, the personal computer 10 has been logging and plotting each resistance and temperature measurement every 2 seconds from steps H, I, J, K, L, M until completion at step N, so that a graph on the screen of the computer 10 will now indicate whether a smooth line transition appears in the up ramp and the down ramp to indicate the integrity and good quality operability of the package.

However, if erratic and non-linear lines appear on the screen of the computer 10, then it is obvious to understand that some type of epoxy short or open circuit has occurred within the package and the package is defective and unsuitable for further use.

Described herein has been a method and apparatus for testing packages of integrated circuit components by programmatically ramping up the temperature a specified amount above room temperature and the ramping down of the device under test (DUT) back to room temperature. This is facilitated by a specially controlled Peltier-junction unit. During the up-ramp and down-ramp cycles, the resistance from power bus to ground is measured and plotted on a computer screen to form a pattern which will indicate component integrity on the one hand, or else the existence of a short circuit or open circuit in one or more components of the package.

Advantageously, a sealed package of internal components can be tested without opening or destroying the package while accomplishing the test checkout in less than 15 minutes.

While a preferred embodiment of the invention has been described, it should be understood that other variations and embodiments may be applied, but which are still encompassed by the attached claims.

WHAT IS CLAIMED IS:

1. A method for testing a multi-chip package in order to test for intermittent or permanent short circuits in the internal components comprising the steps of:

(a) applying a rising temperature to the device under test while concurrently measuring the power bus to ground resistance during an up temperature ramp;

(b) incrementally reducing down the temperature of said device under test back to starting room temperature while monitoring and reading the power bus to ground resistance of the device;

(c) plotting a graph of the power bus to ground resistance of the device during the temperature up ramp and during the temperature down ramp.

2. The method of claim 1 which includes the step of:

(d) noting the regularity or irregularity of the up ramp and down ramp temperature graphs plotted against the power bus to ground resistance in order to determine the operability of components within the multi-chip package.

3. A method for testing internal components of an integrated circuit package having an internal power bus, said method comprising the steps of:

(a) cycling the ambient temperature around said integrated circuit package from room temperature up to a higher selected temperature and then back again to room temperature;

(b) reading out the power bus-ground resistance at selected intervals during the up-ramp temperature change and during the down-ramp temperature change;

(c) plotting a graph of the power bus-ground resistance against temperature during the up-ramp and down-ramp temperature change.

(d) observing the plotted graph to discern a substantially linear resistance change to indicate a normal operating set of components in the integrated circuit package.

4. The method of claim 3 wherein step (d) includes the step of:

(d1) observing an erratic characteristic of the plotted graph to indicate an inoperative component that is shorted or open-circuited.

5. The method of claim 3 wherein step B includes the step of:

(b1) controlling a Peltier-junction module to act as an increasing heat source or as a decreasing heat sink.

6. A method for testing the integrity of internal components of an integrated circuit package having an internal power bus, comprising the steps of:

(a) setting a metallic transfer block unit at a normal room temperature;

(b) attaching a device under test to said transfer block and connecting said power bus-to ground connections internal connections of said device under test to a digital multimeter;

(c) utilizing a computer program for sequencing the temperature of said device under test into an upward temperature rise and subsequently into a downward temperature drop back to room temperature, while concurrently reading the power bus-to ground resistance every 2 seconds during the up-ramp cycle and the down-ramp cycle;

(d) plotting, on a computer screen, the said resistance readings during the up-ramp temperature cycle and the down-ramp temperature cycle;

(e) reading the plotted graph on said computer screen of the power bus-to ground resistance against the temperature up-ramp and down-ramp cycles in order to differentiate a normal set of workable components in said integrated circuit package in order to differentiate inoperable open-circuited or short-circuited components within said integrated circuit module.

7. An apparatus for testing internal components of an integrated circuit package, having an internal power bus, to determine normal operation or problem areas in said components, comprising:

(a) means for temperature cycling said package over a range of 20 degrees Celsius without opening up said package;

(b) means for logging a graph of said power bus to ground resistance against the temperature during the temperature cycle;

(c) means for analyzing said graph to determine normal operation or problem areas in said package.

8. The apparatus of claim 7 wherein said means for temperature cycling includes:

(a1) a computer generated sequencing program to control a Peltier thermoelectric module to act as a heat source and/or heat sink to said package under test.

9. The apparatus of claim 8 wherein said means for logging includes:

(b1) a computer program which graphs and logs the temperature and power bus to ground resistance every 2 seconds during the temperature cycling of said package under test.

10. An apparatus for testing internal components of an integrated circuit package device under test to determine normal operation or problem areas in the components, said apparatus comprising:

(a) test socket means for connecting the device under test with a digital multimeter in order to measure the power bus-to ground resistance of the internal components;

(b) temperature transfer block means connected to a temperature meter for placement adjacent said device under test in order to increase the ambient heat or decrease the ambient heat to said device under test;

(c) a Peltier-thermal electric module adjunct said transfer block means and connected to a programmable power supply for controlling the addition of heat to or reduction of heat from said temperature transfer block;

(d) heat sink and fan means placed adjunct to said Peltier thermal electric module and connected to a controlled fan power supply;

(e) computer means having a control program for connection and management of said controlled fan power supply, said programmable power supply and for sensing operations of said temperature meter and said digital multimeter to controllably enable the sequencing of an up-ramp temperature and a down ramp temperature adjacent said device under test, while concurrently reading-out and plotting the power bus-to ground voltage during the up-cycle and down-cycle of the temperature applied to said device under test.

ABSTRACT OF THE DISCLOSURE:

TITLE: METHOD FOR TESTING MULTI-CHIP PACKAGES

A specialized computer program is utilized to operate apparatus for testing internal components of an integrated circuit package. A Peltier-junction module is controlled so as to ramp-up and ramp-down the temperature of an integrated circuit package while reading out and plotting the power-bus-ground resistance of the package during the up-ramp and down-ramp cycles. The computer screen then indicates a characteristic graph for a properly working package and erratic graph for a package having a short circuit or open circuit components.

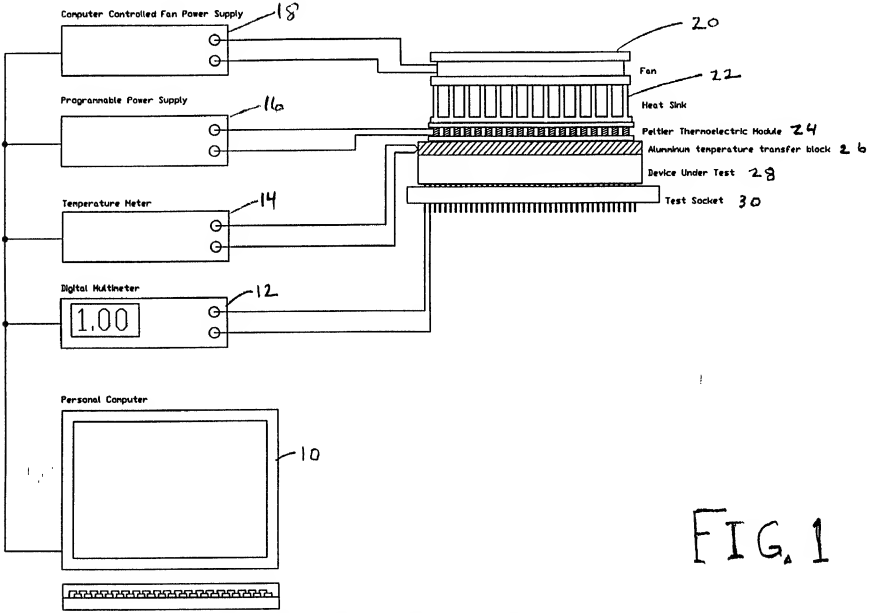
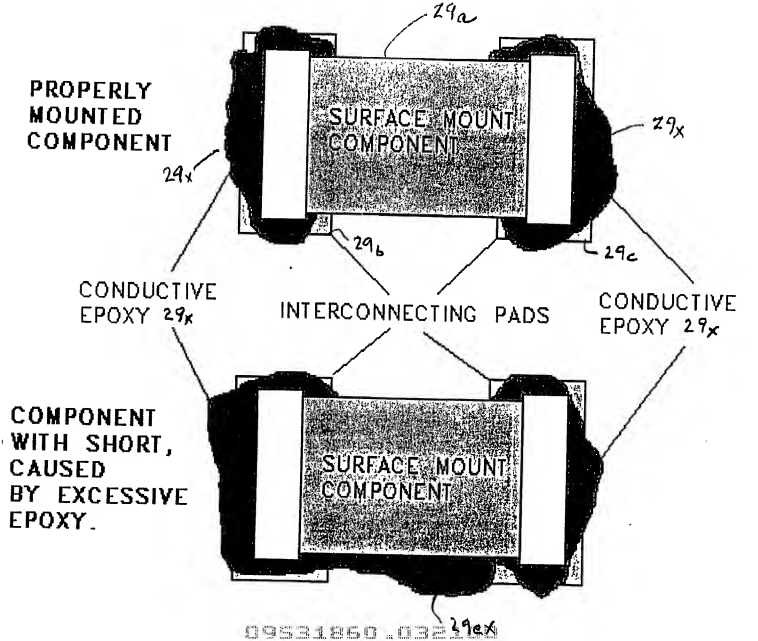


FIG. 1

FIG. 2A



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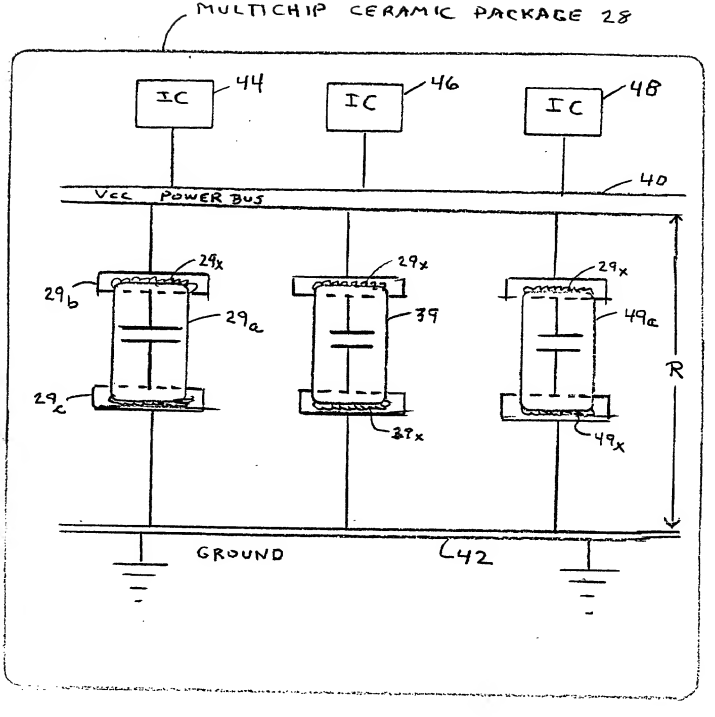

R = measured resistance during temperature ramp-up and ramp-down

FIG. 2B

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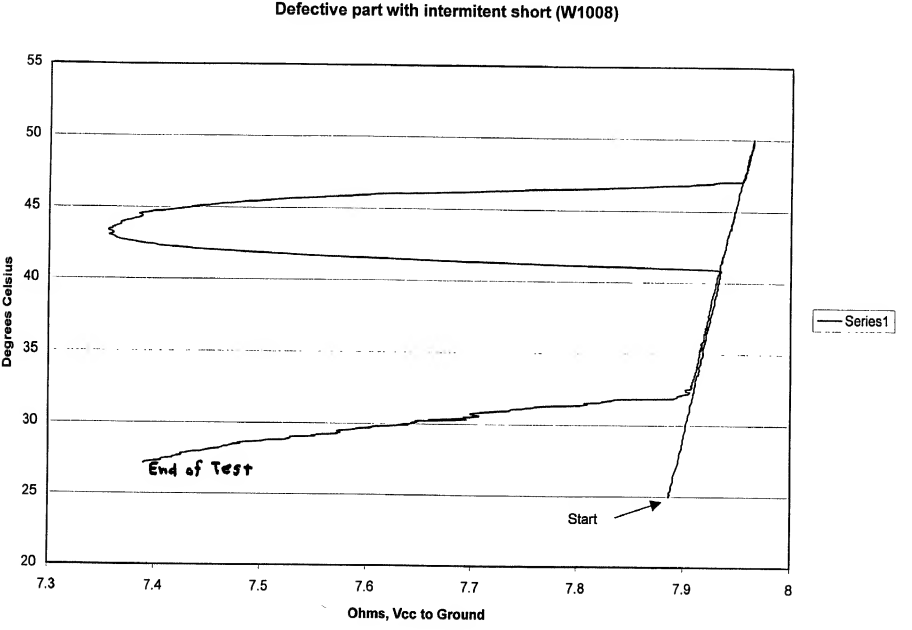

FIG. 3A

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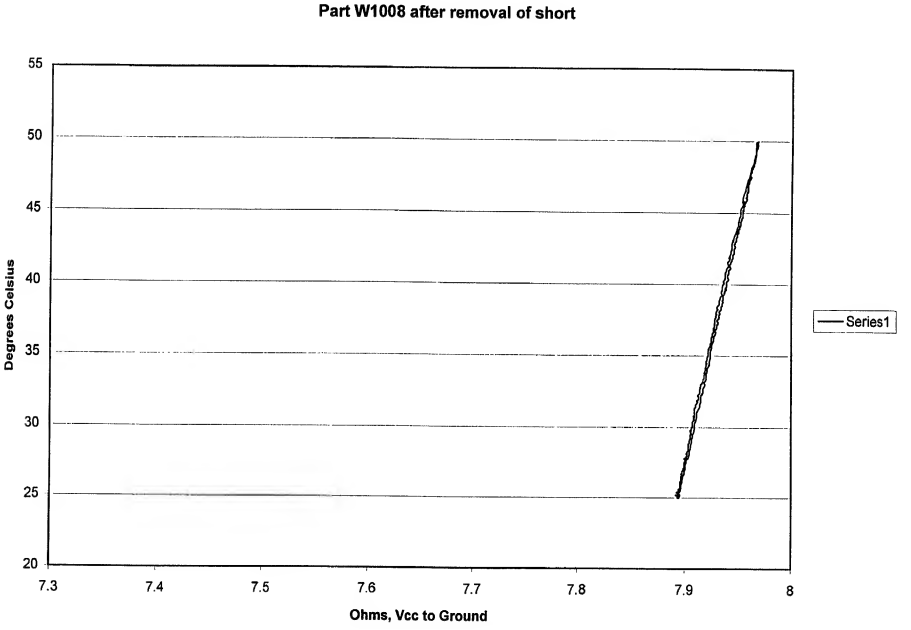

FIG. 3B

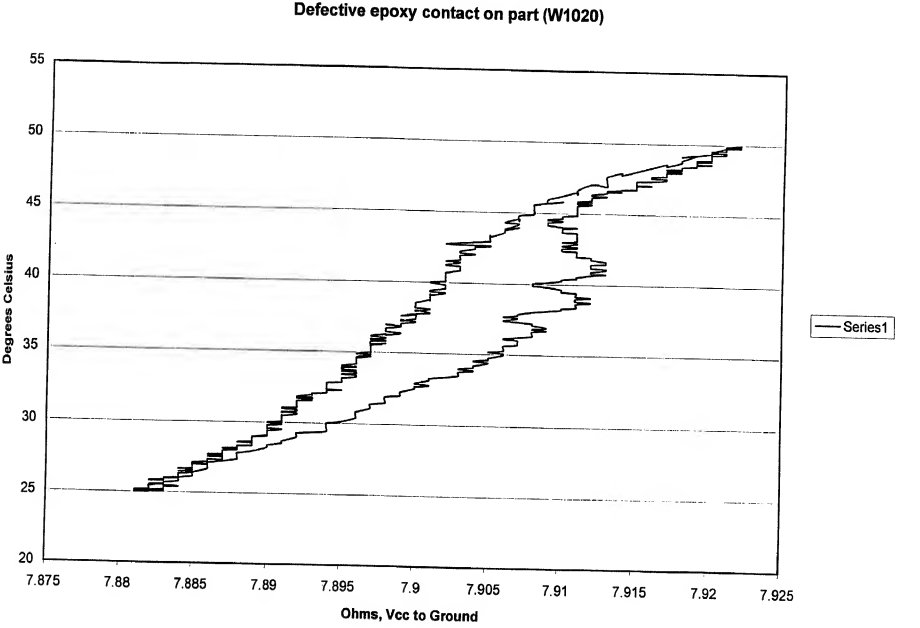

FIG. 4

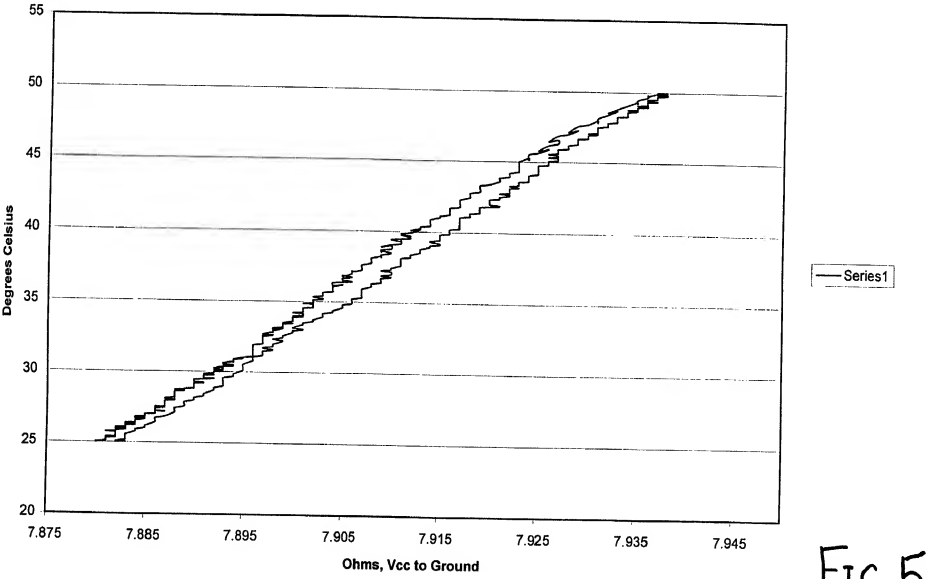

FIG. 5

DKT 481-RB

Attorney's Docket No. 041-481-RB

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is of the following type:

X original

_ design

_ supplemental

_ divisional

_ continuation

_ continuation-in-part (CIP)

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which are a patent is sought on the invention entitled:

TITLE OF INVENTION

METHOD FOR TESTING MULTI-CHIP PACKAGES

SPECIFICATION IDENTIFICATION

the specification of which: (complete (a), (b) or (c))

(a) X is attached hereto.

(b) _was filed on _____ as ☐ Serial No.
or ☐ Express Mail No., as Serial No. not yet known

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment referred to above.

I acknowledge the duty to disclose information

- which is material to patentability as defined in 37, Code of Federal Regulations, § 1.56
- and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable examiner would consider it important in deciding whether to allow the application to issue as a patent, and

___ In compliance with this duty there is attached an information disclosure statement in accordance with 37 CFR 1.98.

POWER OF ATTORNEY

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

ALFRED W. KOZAK, REG. NO. 24,265
MARK T. STARR, REG. NO. 28,762

SEND CORRESPONDENCE TO	DIRECT TELEPHONE CALLS TO: (Name and telephone number)
ALFRED W. KOZAK UNISYS CORPORATION 10850 VIA FRONTERA, MS 1000 SAN DIEGO, CALIFORNIA 92127	ALFRED W. KOZAK (858) 451-4615

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

Full name of sole or first inventor Jorge Humberto Figueredo

Jorge	Humberto	Figueredo
(GIVEN NAME)	(MIDDLE INITIAL OR NAME)	FAMILY (OR LAST NAME)

Inventor's signature  JORGE H. FIGUEREDO

Date 3/21/00 Country of Citizenship Mexico

Residence: 1397 Max Avenue, Chula Vista, California 91911

Post Office Address same as above